

BB-AN-0004

Integrating SwitchBlox Nano, Harwin variant with an RJ-45 Jack

Application Note

January 2024



1 Introduction

SwitchBlox Nano comes in a board mountable version that allows it to be integrated directly into a customer board. A common use case is for the ports on SwitchBlox Nano to be directly connected to an external RJ-45 jack on a customer board. This application note provides guidance on how to achieve this.

2 Compatible RJ-45 Jacks

SwitchBlox Nano contains the necessary transformers and common mode chokes (collectively referred to as "magnetics" to achieve required galvanic isolation of 2250 VDC as required for IEEE 802.3, therefore you do not need to add any magnetics to your board.

This means you should utilize simple RJ-45 jacks, rather than RJ-45 jacks with integrated magnetics. Use RJ-45 with integrated magnetics (or placing additional magnetics on your board) will reduce signal strength without adding any benefit. The list below provides some examples of compatible RJ-45 jacks that may be used with SwitchBlox Nano.

- TE Connectivity 1761825-1
- Adam Tech MTJ-882BX1
- Pulse Electronics E5J88-00LJG2-L
- Molex 0955012881



3 Example Schematic

Schematic and footprint symbols for BB-SWN-E-1-HW can be downloaded from SnapEDA here. This allows easy integration with nearly all ECAD software including Altium, Kicad and Orcad.

Figure 1 below shows how to connect SwitchBlox Nano to the 1761825-1, which is a three port RJ-45 jack connector without magnetics.

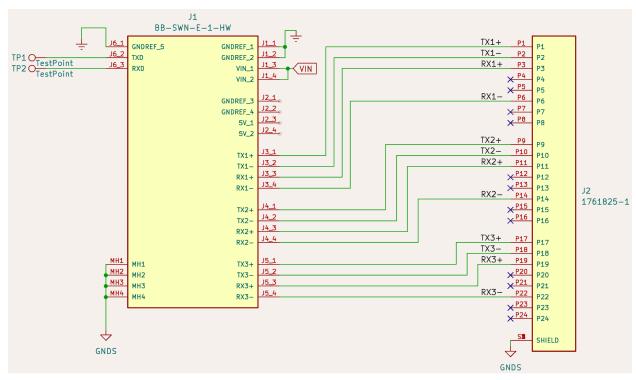


Figure 1 - Connecting SwitchBlox Nano Harwin Variant to the 1761825-1 three port RJ-45 jack.

Note that SwitchBlox Nano uses 10/100BASE-T ethernet, which only requires four pins, whereas an RJ-45 jack has eight pins. This is because RJ-45 jacks need to be able to accommodate 1000BASE-T (and higher) ethernet, which uses all eight pins. In the case of 10/100BASE-T, you only need to connect four pins of the RJ-45 jack.

The specific pins to connect on the RJ-45 jack are determined by T-568A wiring, which uses the following mapping

Pin 1: TX+ Pin 2: TX-Pin 3: RX+ Pin 6: RX-

Figure 2 below shows this visually.



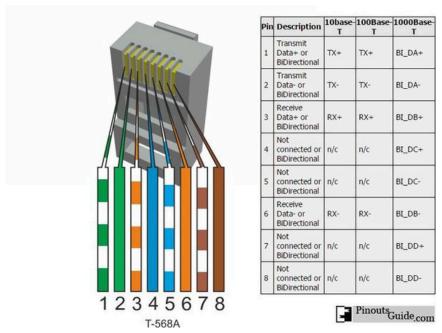


Figure 2 - The pin mapping of an RJ-45 under the T-568A pin scheme. [Image source - pinoutsguide.com]

Based on this, determining the pins to connect to on the footprint of the RJ-45 jack is usually simple. In most cases, RJ-45 jack footprints name the pins according to this same scheme, but not always. As such, it is always suggested to visually check the orientation of the RJ-45 plug to figure out which pin is pin 1 in the footprint.

You do not need any other components between SwitchBlox Nano and your RJ-45 jack. Note that the shield of the RJ-45 jack is not connected to the ground pin of SwitchBlox Nano. Typically the shield of the RJ-45 jack connects directly with the external chassis, and is often galvanically separated from the voltage rails used inside the device.

Note that all ports on SwitchBlox Nano are equal, and thus you can select whatever specific port to RJ-45 jack mapping best suits layout needs.

4 Example PCB Layout

To improve layout, the schematic in figure 1 was modified, moving the ports around to make layout easier. The amended schematic in figure 3 shows this. Note that there is no functional difference between this and the previous mapping, other than a difference in port numbering.

Figure 4 shows the finished layout.



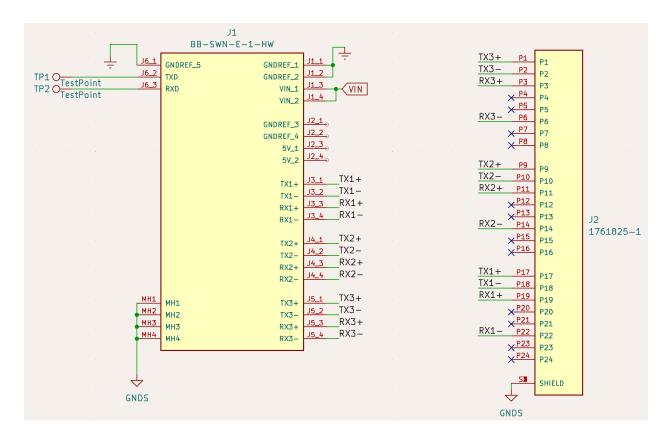


Figure 3 - An amended schematic that swapped the position of ports 1 and 3 on the RJ-45 jacks to improve layout



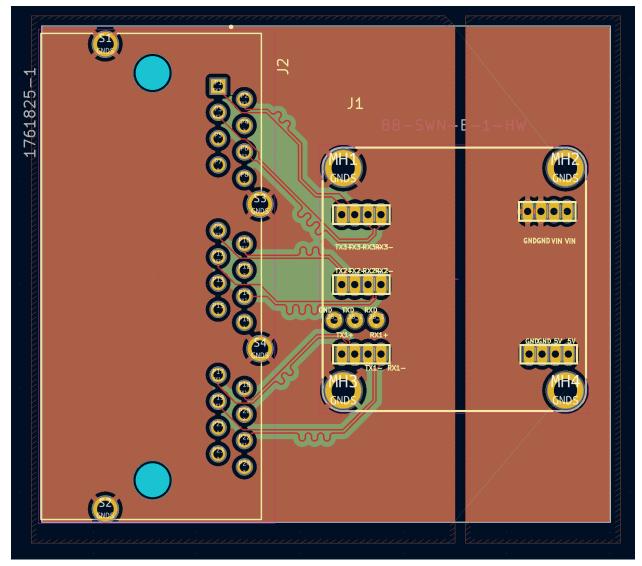


Figure 4 - The final layout, showing the ethernet traces with matched skew.

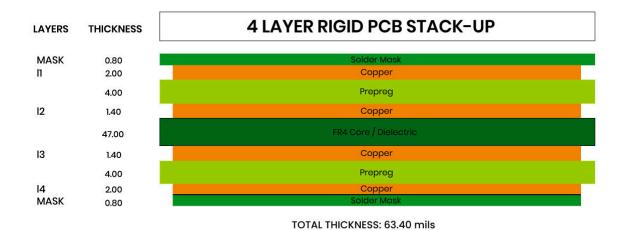
The differential pairs must maintain a 1000hm differential impedance on your board. We recommend using the same stackup and design rules as used on SwitchBlox Nano, listed below.

Differential pair, track width: 0.1524mmDifferential pair, spacing: 0.1524mm

Via size: 0.6mmVia drill: 0.3mm

• Stackup: 4 layer PCB, FR4 dielectric as below





Notes: Outer layer copper thickness is 1/2 oz before plating. Finished outer layer CU thickness is approximately 1.4 to 2.2 mils after plating.

Figure 5 - Suggested stackup for customer board. Using a different stackup may mean you need to adjust your differential pair track width and spacing to maintain a 1000hm differential impedance.



5 Datasheet Changelog

Date	Datasheet Version	Author	Notes
20/01/2024	A_A	Josh Elijah	Initial release

6 Contact

If you have any questions regarding this product, please contact us:

info@botblox.org 4 Pavilion Court 600 Pavilion Drive, Northampton Business Park, Northampton, England NN4 7SL